

## CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

- 1    1. A free-standing compliant off-chip interconnect, comprising:
  - 2       a first arcuate structure;
  - 3       a second arcuate structure, wherein the first arcuate structure and the second
  - 4       arcuate structure are disposed in substantially parallel planes; and
  - 5       a middle post, wherein the first arcuate structure is connected to a lower portion of
  - 6       the middle post, and wherein the second arcuate structure is connected to an upper
  - 7       portion of the middle post.
- 1    2. The compliant off-chip interconnect of claim 1, wherein the first arcuate structure
- 2       has a first mean radius and the second arcuate structure has a second mean radius,
- 3       wherein the first mean radius and the second mean radius are not equivalent.
- 1    3. The compliant off-chip interconnect of claim 1 wherein the first arcuate structure
- 2       has a first mean radius and the second arcuate structure has a second mean radius,
- 3       wherein the first mean radius and the second mean radius are equivalent.
- 1    4. The compliant off-chip interconnect of claim 1, wherein the first arcuate structure
- 2       has a thickness of about 3 to about 30 micrometers, a width of about 5 to about 50
- 3       micrometers, and a mean radius of about 5 to about 100 micrometers.

1    5.      The compliant off-chip interconnect of claim 1, wherein the second arcuate  
2      structure has a thickness of about 3 to about 30 micrometers, a width of about 5 to about  
3      50 micrometers, and a mean radius of about 5 to about 50 micrometers.

1    6.      The compliant off-chip interconnect of claim 1, wherein the middle post has a  
2      height of about 5 to about 50 micrometers.

1    7.      The compliant off-chip interconnect of claim 1, further comprising:  
2                a substrate upon which the first arcuate structure and the second arcuate structure  
3                are disposed.

1       8.     A electronic package comprising:  
2              a substrate; and  
3              a free-standing compliant off-chip interconnect, wherein the free-standing  
4     compliant off-chip interconnect includes a first free-standing arcuate structure that is  
5     substantially parallel to the substrate.

1       9.     The electronic package of claim 8, wherein the free-standing compliant off-chip  
2     interconnect further includes:  
3              a second free-standing arcuate structure that is substantially parallel to the  
4     substrate, and wherein the first arcuate structure and the second arcuate structure are  
5     disposed in substantially parallel planes.

1       10.    The electronic package of claim 8, wherein the first arcuate structure is connected  
2     to an assembly post.

1       11.    The electronic package of claim 8, wherein the first arcuate structure is connected  
2     to an assembly post with a first bridge.

1       12.    The electronic package of claim 11, wherein the first bridge includes a curved  
2     portion connecting the first arcuate structure to the assembly post.

1       13.    The electronic package of claim 9, wherein the second arcuate structure is  
2     connected to a fabrication post with a second bridge.

1    14.    The electronic package of claim 13, wherein the second bridge includes a curved  
2    portion connecting the second arcuate structure to the fabrication post.

1    15.    The electronic package of claim 8, wherein the first arcuate structure has a  
2    thickness of about 3 to about 30 micrometers, a width of about 5 to about 50  
3    micrometers, and a mean radius of about 5 to about 100 micrometers.

1    16.    The electronic package of claim 9, wherein the second arcuate structure has a  
2    thickness of about 3 to about 30 micrometers, a width of about 5 to about 50  
3    micrometers, and a mean radius of about 5 to about 100 micrometers.

1    17.    The electronic package of claim 8, wherein the assembly post has a height of  
2    about 5 to about 50 micrometers.

1    18.    The electronic package of claim 9, wherein the first arcuate structure has a first  
2    mean radius and the second arcuate structure has a second mean radius, wherein the first  
3    mean radius and the second mean radius are not equivalent.

1    19.    The electronic package of claim 9, wherein the first arcuate structure has a first  
2    mean radius and the second arcuate structure has a second mean radius, wherein the first  
3    mean radius and the second mean radius are equivalent.

- 1    20.    The electronic package of claim 8, wherein the substrate can be a material chosen
- 2    from a semiconductor, glass, ceramic, and quartz material.

1    21.    A method of fabricating a free-standing arcuate structure compliant off-chip  
2    interconnect, the method comprising:  
3        depositing an arcuate structure compliant off-chip interconnect material; and  
4        forming the free-standing arcuate structure compliant off-chip interconnect.

1    22.    The method of claim 21, wherein depositing an arcuate structure compliant off-  
2    chip interconnect material further comprises:  
3        forming a first arcuate structure, wherein the first arcuate structure is substantially  
4        parallel to the substrate.

1    23.    The method of claim 22, wherein depositing an arcuate structure compliant off-  
2    chip interconnect material further comprises:  
3        forming a second arcuate structure, wherein the first arcuate structure and the  
4        second arcuate structure are disposed in substantially parallel planes.

1       24.     The method of claim 22, wherein depositing an arcuate structure compliant off-  
2     chip interconnect material further comprises:  
3                 forming the first arcuate structure having a thickness of about 3 to about 30  
4     micrometers, a width of about 5 to about 50 micrometers, and a mean radius of about 5 to  
5     about 100 micrometers.

1       25.     The method of claim 23, wherein depositing an arcuate structure compliant off-  
2     chip interconnect material further comprises:  
3                 forming the second arcuate structure having a thickness of about 3 to about 30  
4     micrometers, a width of about 5 to about 50 micrometers, and a mean radius of about 5 to  
5     about 100 micrometers.

1       26.     The method of claim 21, wherein the substrate is chosen from semiconductor,  
2     ceramic, glass, and quartz materials.